제20회 한국반도체학술대회

2013년 2월 4일(월)~6일(수) / 웰리힐리파크 (구, 성우리조트)

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K. Memory (Design & Process Technology) 분과

Room E
스타홀 (본관, 2층)

2013년 2월 6일(수) 15:10-16:25
[WE3-K] Nonvolatile Memory Techniques II
좌장: 곽동화(삼성전자), 김용기(SK 하이닉스)

[초청]

WE3-K-1 **15:10-15:40** **Challenge in Development of Resistance Switching Memory**
김수길, 정수옥, 이정훈, 홍성주
SK 하이닉스 연구소 선행소자그룹 선행소자NtI팀

WE3-K-2 **15:40-15:55** **Analysis of Stress-Induced Traps Generation on Random Telegraph Noise for TANOS(TaN-Al_2O_3-Si_3N_4-SiO_2-Si) NAND Flash Memories**
Byeong-In Choe[1,2], Changseok Kang[2], Youngwoo Park[2], Woonkyung Lee[2], Byung-Gook Park[1], and Jong-Ho Lee[1]
[1]School of EECS and ISRC, Seoul National University, [2]Flash TD, Semiconductor R&D Center, Samsung Electronics Co., Ltd.

WE3-K-3 **15:55-16:10** **Channel Selection by Multi Level Operation of String Select Line in 3D Channel Stacked NAND Flash Memory Array**
Wandong Kim, Yoon Kim, Se-Hwan Park, Joo Yun Seo, Do-Bin Kim, Sang-Ho Lee, and Byung-Gook Park
Inter-University Semiconductor Research Center and School of Electrical Engineering and Computer Science, Seoul National University

WE3-K-4 **16:10-16:25** **Relationship between Program Disturb and Initial Erase State for Endurance in NAND Flash Memory**
윤중호, 홍옥천, 김홍식, 우형동, 유원정, 장성진, 김영삼, 박성욱, 김건수, 이규필
삼성전자 제조센터 Yield Enhancement Team