

F. Silicon Device and Integration Technology **분과**

Room G

하나스퀘어 (B112)

일 시 : 2월 16일(목) 11:20-12:35

세션명 : [TG2-F] Integration Technology for Advance Materials and Devices

좌 장 : 이석희(KAIST), 이병훈(광주과학기술원)

-
- TG2-F-1 11:20-11:35 Effect of SC1 Cleaning on the Performance of Graphene FET**
저자: 박은지¹, 강창구², 이상경², 조천흠¹, 이영곤², 정현종³,
서순애⁴, 이병훈^{1,2}
소속: ¹광주과학기술원 나노바이오 전자재료공학과, ²광주과학기술원
신소재공학부, ³삼성종합기술원, ⁴세종대학교 물리학과
- TG2-F-2 11:35-11:50 Wafer-scale Graphene Nanoribbons for Tunnel FET Applications**
저자: W. S. Hwang¹, K. Tahy¹, P. Zhao¹, R. L. Myers-Ward², P. M.
Campbell², C. R Eddy², Jr., D. K. Gaskill², H. Xing¹, A. C.
Seabaugh¹, and D. Jena¹
소속: ¹Department of Electrical Engineering, University of Notre Dame,
²U. S. Naval Research Laboratory
- TG2-F-3 11:50-12:05 The Improvement of Device Characteristic in HK/MG Logic Device by Newly Developed CESL**
저자: Hyunkwan Yu, Yong-kuk Jeong, Pankwi Park, Ki-Eun Kim,
Sang-Uk Park, Dong Suk Shin, Moon Han Park, Ja-Hm Ku,
and Nae-In Lee
소속: Advanced Process Development / TD, System LSI Division,
Samsung Electronics Co., Ltd.
- TG2-F-4 12:05-12:20 The Effect of Thermal Budget on the Insulating Properties of HfO₂ on Ge Substrate**
저자: Hyung-Suk Jung¹, Il-Hyuk Yu¹, Hyo Kyeom Kim¹, Sang Young
Lee¹, Tae Joo Park², Nae-In Lee³, and Cheol Seong Hwang¹
소속: ¹WCU Hybrid Materials Program, Department of Materials
Science and Engineering and Inter-university Semiconductor
Research Center, Seoul National University, ²Hanyang University,
³SYS LSI division, Samsung Electronics Co., Ltd.

- TG2-F-5 12:20-12:35 **Ground-plane Doping for V_T -modulation of Planar Tunnel Field-effect Transistors on Ultra-thin-body and BOX (UTBB) SOI Substrate**
저자: M.-C. Sun^{1,2}, H. Kim¹, S. W. Kim¹, G. Kim¹, H. W. Kim¹, J.-H. Lee¹, H. Shin¹, and B.-G. Park¹
소속: ¹Inter-university Semiconductor Research Center and School of Electrical Engineering and Computer Science, Seoul National University, ²TD (S. LSI), Semiconductor Business Group, Samsung Electronics Co., Ltd.