G. Device & Process Modeling, Simulation and Reliability 분과

Room G
하나스퀘어 (B112)

일 시 : 2월 17일(금) 13:40-15:10
세션명 : [FG3_G] Device Performance & Reliability Issues in Non-Volatile Memories and Advanced Devices
좌 장 : 최재훈(하이닉스반도체), 이재규(삼성전자)

FG3_G-1 13:40-14:10 [Invited]Development of Stress Memorization Technique Applicable for 20nm Low Power SoC Process

저자: Choongryul Ryou[1], Sang-Su Kim[2], Yaoqi Dong[1], ByoungGi Kim[1], Weon-wi Jang[1], Seunghyun Song[3], Hongseon Yang[3], Uihui Kwon[3], Youngdal Lim[1], Soohun Hong[1], Yoonmoon Park[1], Sada-aki Masuoka[1], Jae Gon Lee[1], Dong-Won Kim[1], Sang-Pil Sim[1], Dong Kyun Sohn[1], Jong Shik Yoon[1] and Chilhee Chung[1]
소속: [1]Logic TD Team, Semiconductor R&D division, Samsung Electronics Co., Ltd., [2]Process Development P/J3, Semiconductor R&D division, Samsung Electronics Co., Ltd., [3]CAE Team, Semiconductor R&D division, Samsung Electronics Co., Ltd.

FG3_G-2 14:10-14:25 Improvement of Electrical Overstress Robustness of GGNMOS I/O Cells for Timing Controller Application

저자: Yon-Sup Pang, Youngju Kim, Jinseop Shim, Young-Chul Kim, Taehoon Kim, Kyongjin Hwang, Hyun-Ho Jang, Sookjin Kwon, Leeyeun Hwang, Sung-Bum Park, and Taejong Lee
소속: NVM/Device/ESD, DSD KDC and LDDI PE Teams, MagnaChip Semiconductor

FG3_G-3 14:25-14:40 Write Margin Variability and V_{CCmin} projection of 6T SRAM with Double-Gate MOSFETs down to Lmin=8nm

저자: Boung Jun Lee and Ji-Woon Yang
소속: Department of Electronics and Information Engineering, Korea University

FG3_G-4 14:40-14:55 Analysis of Single Poly EEPROM Characteristics on the Multiple Doped

Floating Gate Structure

저자: JN Eum, YJ Kwon, SK Park, SH Lee, KS Ko, DH Kim, KS Lee, IW Cho, and KD Yoo
소속: TD Team, M8 Division, Hynix Semicondutor Inc.

FG3_G-5 14:55-15:10

Amorphous Silicon 박막트랜지스터의 Negative Bias Illumination Stress 하에서의 물리적 Parameter 기반 신뢰성 특성분석

저자: 정현광, 공동식, 김용식, 배민경, 김재형, 김우준, 허인석, 이재욱, 김윤혁, 전성우, 조춘형, 김동명, 김대환
소속: School of Electrical Engineering, Kookmin University